

Recent Single Event Effects Compendium of Candidate Electronics for NASA Space Systems

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Abstract— We present the results of single event effects (SEE) testing and analysis investigating the effects of radiation on electronics. This paper is a summary of test results.

Index Terms—Single event effects, spacecraft electronics, digital, linear bipolar, and hybrid devices.

I. INTRODUCTION

The performance of electronic devices in a space radiation environment is often limited by its susceptibility to SEE. Interpreting the results of SEE testing of complex devices is quite difficult. Given the rapidly changing nature of both technology and the related SEE issues being discovered, SEE test data is very application specific and adequate understanding of the test conditions is critical [1].

Given this limitation of test data (application-specific), studies discussed herein were undertaken to establish the sensitivities of candidate spacecraft electronics as well as new electronic devices to heavy ion and proton-induced single event upset (SEU), single event latchup (SEL), and single event transients (SET). For total ionizing dose (TID) and displacement damage (DD) results, see a companion paper submitted to the 2011 IEEE NSREC Radiation Effects Data Workshop entitled: "Recent Total Ionizing Dose and

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Displacement Damage Compendium of Candidate Electronics for NASA Space Systems" by D. Cochran, *et al.* [2].

II. TEST TECHNIQUES AND SETUP

A. Test Facilities

All SEE tests were performed between February 2010 and February 2011. Heavy ion experiments were conducted at Lawrence Berkeley National Laboratory (LBNL) [3], and at Texas A&M University Cyclotron (TAMU) [4]. Both of these facilities are suitable for providing a variety of ions over a range of energies for testing. The devices under test (DUTs) were irradiated with heavy ions having linear energy transfers (LETs) ranging from 0.59 to 120 MeV·cm²/mg. Fluxes ranged from 1×10² to 1×10⁷ particles/cm²/s, depending on device sensitivity. Representative ions used are listed in Table I. LETs between the values listed were obtained by changing the angle of incidence of the ion beam with respect to the DUT, thus changing the path length of the ion through the DUT and the "effective LET" of the ion [5]. Energies and LETs available varied slightly from one test date to another.

Proton SEE tests were performed at three facilities: the University of California at Davis (UCD) Crocker Nuclear Laboratory (CNL) [6], the Indiana University Cyclotron Facility (IUCF) [7], and at a 2 MeV Van de Graaff (VdG) particle accelerator. Proton test energies incident on the DUT are listed in Table II.

Laser SEE tests were performed at the pulsed laser facility at the Naval Research Laboratory (NRL) [8] [9]. The laser light had a wavelength of 590 nm resulting in a skin depth (depth at which the light intensity decreased to 1/e - or about 37% - of its intensity at the surface) of 2 μm. A nominal pulse rate of 1 kHz was utilized.

TABLE I: HEAVY ION TEST FACILITIES AND TEST HEAVY IONS

	Ion	Energy (MeV)	Surface LET in Si (MeV·cm ² /mg) (Normal Incidence)	Range in Si (μm)
LBNL	¹⁸ O	184	2.2	227
	²² Ne	216	3.5	175
	⁴⁰ Ar	400	9.7	130
	⁶⁵ Cu	659	21	110
	⁸⁶ Kr	886	31	110
	¹³⁶ Xe	1330	59	97
10 MeV per AMU tune				
TAMU	²⁰ Ne	300	2.5	316
	⁴⁰ Ar	599	7.7	229
	⁶³ Cu	944	17.8	172
	⁸⁴ Kr	1259	25.4	170
	¹⁰⁹ Ag	1634	38.5	156
	¹²⁹ Xe	1934	47.3	156
	15 MeV per AMU tune			
	²² Ne	545	1.8	799
	⁴⁰ Ar	991	5.5	493
	⁸⁴ Kr	2081	19.8	332
	¹³⁹ Xe	3197	38.9	286
25 MeV per AMU tune				

TABLE II: PROTON TEST FACILITIES

University of California at Davis (UCD) Crocker Nuclear Laboratory (CNL), energy tunes ranged from 6.5 to 63 MeV, flux ranged from 8×10^7 to 1×10^9 particles/cm ² /s.
Indiana University Cyclotron Facility (IUCF), energy ranged from 63 to 198 MeV, flux ranged from 5×10^5 to 3×10^9 particles/cm ² /s.

TABLE III: LASER TEST FACILITY

Naval Research Laboratory (NRL) Pulsed Laser SEE Test Facility Laser: 590 nm, 1 ps pulse width, beam spot size ~1.2 μm

B. Test Method

Unless otherwise noted, all tests were performed at room temperature and with nominal power supply voltages. We recognize that high-temperature and worst-case power supply conditions are recommended for single event latchup (SEL) device qualification.

1) SEE Testing - Heavy Ion:

Depending on the DUT and the test objectives, one or more of three SEE test methods were typically used:

Dynamic – the DUT was exercised continually while being exposed to the beam. The events and/or bit errors were counted, generally by comparing the DUT output to an unirradiated reference device or other expected output (Golden chip or virtual Golden chip methods) [10]. In some cases, the effects of clock speed or device operating modes were investigated. Results of such tests should be applied with caution due to the application-specific nature of the results.

Static – the DUT was loaded prior to irradiation; data were retrieved and errors were counted after irradiation.

Biased – the DUT was biased and clocked while power consumption was monitored for SEL or other destructive effects. In most SEL tests, functionality was also monitored.

In SEE experiments, DUTs were monitored for soft errors, such as SEUs and for hard errors, such as single event gate rupture (SEGR). Detailed descriptions of the types of errors observed are noted in the individual test reports [11],[12].

SET testing was performed using a high-speed oscilloscope controlled via Labview®. Individual criteria for SETs are specific to the device being tested and application. Please see the individual test reports for details [11].

Heavy ion SEE sensitivity experiments include measurement of the Linear Energy Transfer threshold (LET_{th}) and cross section at the maximum measured LET. The LET_{th} is defined as the maximum LET value at which no effect was observed at an effective fluence of 1×10^7 particles/cm². In the case where events are observed at the smallest LET tested, LET_{th} will either be reported as less than the lowest measured LET or determined approximately as the LET_{th} parameter from a Weibull fit. In the case of SEGR experiments, measurements are made of the SEGR threshold V_{ds} as a function of LET at a fixed V_{gs} .

2) SEE Testing - Proton

Proton SEE tests were performed in a manner similar to heavy ion exposures. However, because protons cause SEE via indirect ionization of recoil particles, results are parameterized in terms of proton energy rather than LET. Because such proton-induced nuclear interactions are rare, proton tests also feature higher cumulative fluences and particle flux rates than heavy ion experiments.

3) Pulsed Laser Facility Testing

The DUT was mounted on an X-Y-Z stage in front of a 100x lens that produced a spot diameter of about 1.2 μm at full-width half-maximum (FWHM). The X-Y-Z stage can be moved in steps of 0.1 μm for accurate positioning of SEU sensitive regions in front of the focused beam. An illuminator together with a charge coupled device camera and monitor were used to image the area of interest, thereby facilitating accurate positioning of the device in the beam. The pulse energy was varied in a continuous manner using a polarizer/half-waveplate combination and the energy was monitored by splitting off a portion of the beam and directing it at a calibrated energy meter.

III. TEST RESULTS OVERVIEW

Abbreviations and conventions are listed in Table IV. Abbreviations for principal investigators (PIs) are listed in Table V, and SEE results are summarized in Table VI. Unless otherwise noted, all LETs are in MeV·cm²/mg and all cross sections are in cm²/device. All SEL tests are performed at a fluence of 1×10^7 particles/cm² unless otherwise noted.

TABLE IV: ABBREVIATIONS AND CONVENTIONS

LET = linear energy transfer ($\text{MeV}\cdot\text{cm}^2/\text{mg}$)
 LET_{th} = linear energy transfer threshold (the maximum LET value at which no effect was observed at an effective fluence of 1×10^7 particles/ cm^2 – in $\text{MeV}\cdot\text{cm}^2/\text{mg}$)
 $< =$ SEE observed at lowest tested LET
 $> =$ no SEE observed at highest tested LET
 σ = cross section ($\text{cm}^2/\text{device}$, unless specified as cm^2/bit)
 $\sigma_{\text{max measured}}$ = cross section at maximum measured LET ($\text{cm}^2/\text{device}$, unless specified as cm^2/bit)
 ADC = analog to digital converter
 App. Spec. = application specific
 ASET = analog single-event transient
 BiCMOS = bipolar complementary metal oxide semiconductor
 CMOS = complementary metal oxide semiconductor
 DAC = digital to analog converter
 DTMR = distributed triple modular redundancy
 DUT = device under test
 EDAC = error detection and correction
 FPGA = field programmable gate array
 GaAs = gallium arsenide
 H = heavy ion test
 InGaP = indium gallium phosphide
 L = laser test
 LBNL = Lawrence Berkeley National Laboratory
 LCDT = low cost digital tester
 LC^2MOS = linear compatible CMOS (LC^2MOS) process
 LDC = lot date code
 LO = local oscillator
 LTMR = localized triple modular redundancy
 MDAC = multiplying digital-to-analog converter
 MESFET = metal semiconductor field effect transistor
 MMIC = microwave monolithic integrated circuit
 MOSFET = metal oxide semiconductor field effect transistor
 MSOP = mini small outline package
 NA = not available
 NRL = Naval Research Laboratory
 P = proton test (SEE)

PCM = phase change memory

Table IV: Abbreviations and Conventions (Cont.)

PI = principal investigator
 PN = part number
 POL = point of load
 SEB = single event burnout
 SEE = single event effect
 SEFI = single event functional interrupt
 SEGR = single event gate rupture
 SEL = single event latchup
 SET = single event transient
 SEU = single event upset
 SiGe = silicon germanium
 VdG = Van de Graaff
 VDMOS = drain voltage MOSFET
 V_{ds} = drain-source voltage
 V_{gs} = gate-source voltage
 V_{th} = gate threshold voltage
 WC = worst case

TABLE V: LIST OF PRINCIPAL INVESTIGATORS

Principal Investigator (PI)	Abbreviation
Melanie Berg	MB
Michael Campola	MiC
Dakai Chen	DC
Hak Kim	HK
Jean-Marie Lauenstein	JML
Timothy Oldham	TO
Jonathan Pellish	JP
Anthony (Tony) Sanders	AS
Michael Xapsos	MX

TABLE VI: SUMMARY OF SEE TEST RESULTS

Part Number	Manufacturer	LDC	Device Function	Tech-nology	Particle: (Facility/Date) P.I.	Test Results LET in $\text{MeV}\cdot\text{cm}^2/\text{mg}$ or in $\text{cm}^2/\text{device}$, unless otherwise specified	Supply Voltage	Sample Size (Number Tested)	Reference
ADC/DAC:									
AD7847	Analog Devices	0801A	DAC	BiCMOS	H: (TAMU10DEC) JP	H: SEL $\text{LET}_{\text{th}} > 82$ @ 65°C	+/- 15V	3	[13]
ADS7881	Texas Instruments	1010	ADC	CMOS	H: (TAMU10OCT) JP	H: SEL $\text{LET}_{\text{th}} > 77$ @ 65°C	+/- 5V	4	[14]
LTC1864L	Linear Technology	9D17	16-bit ADC	MSOP CMOS	H: (TAMU10AUG) MB	H: SEL $\text{LET}_{\text{th}} < 3.96$; 1.0 < SEU $\text{LET}_{\text{th}} < 2.8$	3.3V I/O; 1.5V Core	3	[15]
AD7872 (Generic PN); 7872ARPS (Package PN)	Analog Devices (Maxwell Package)	1008	14-bit ADC	LC^2MOS	H: (TAMU10FEB) MiC	H: SEL $\text{LET}_{\text{th}} > 59.2$ @ 70°C ; SEU $\text{LET}_{\text{th}} < 8.8$; SET $\text{LET}_{\text{th}} < 2.9$; Transient pulse amplitude > 10mV.	5V	3	[16]
DC-DC Converter/POL:									
PE9915X	Peregrine Semiconductor	S11060-2; S11058-2	Step down switching regulator	CMOS SOS	H: (LBNL11JAN) DC	H: SEL/SEGR/SEB $\text{LET}_{\text{th}} > 118$ @ room temperature.	5V	3	[17]
MSK5059RH	M. S. Kennedy	MSK 5059RHG Be0 51651 USA	Step down switching regulator	BiCMOS	H: (TAMU10DEC; TAMU11JUN) DC	H: SEL/SEGR/SEB $\text{LET}_{\text{th}} > 87.5$ @ room temperature; Further tests pending.	7V	3	[18]
MSK5820	Linear Technology	1014	Linear Voltage Regulator	Hybrid	H: (TAMU10MAY) MiC	H: SET $\text{LET}_{\text{th}} < 2.9$; Typically SET $\sim 70\text{us}$, 70mV; WC transient $\sim 180\text{us}$, 100mV.	5V	2	[19]
SMRT28515T	Crane	0824	DC-DC Converter	Hybrid	H: (TAMU10MAR; LBNL10JUN; TAMU10NOV) AS	H: SEL $\text{LET}_{\text{th}} > 86.3$; SET $\text{LET}_{\text{th}} < 25$; SETs observed at $\sim \pm 300\text{mV}$ peak, 600ns.	+/-15V	1	[20]

Part Number	Manufacturer	LDC	Device Function	Technology	Particle: (Facility/Date) P.I.	Test Results LET in MeV·cm ² /mg or in cm ² /device, unless otherwise specified	Supply Voltage	Sample Size (Number Tested)	Reference
SMTR283R3S	Crane	0733; 0408; 0722	DC-DC Converter	Hybrid	H: (TAMU10MAR; TAMU10NOV) AS	H: SEL LET _{th} > 86.3; SET LET _{th} < 54; SETs observed at ~700mV peak, 100us.	3.3V	3	[21] [22]
SMSA2812D	Crane	0733	Dual DC-DC Converter	Hybrid	H: (TAMU10MAR; TAMU10NOV) AS	H: SEL LET _{th} > 86.3; SET LET _{th} < 28.8; SETs observed at ~+/-300mV peak to peak, 700us;	+/-12V	2	[23] [24]
MFP0507S	Crane	LDC Not Released; markings 0077; 0078; 0082; 0083	DC-DC Converter	Hybrid	H: (TAMU10DEC; LBNL11JAN) AS	H: SEL LET _{th} > 85.4; SET LET _{th} < 3.49; SETs at 0.8V were ~200mV, 100us; at 3.3V SETs were <800mV, 200us.	.8V; 3/3V	4	[25] [26]
SLH2812D	Crane	0748	Dual DC-DC Converter	Hybrid	H: (LBNL10JUN; TAMU10NOV; TAMU10MAR) AS	H: SEL LET _{th} > 86.3; SET LET _{th} < 58.8; SETs observed at ~1V peak, 700ns.	+/-12V	3	[27] [28]
SMFLHP2815S	Crane	0623	DC-DC Converter	Hybrid	H: (TAMU10MAR; TAMU10NOV) AS	H: SEL LET _{th} > 86.3; SET LET _{th} < 53.1; SETs observed at ~1V peak, 200us.	+/-15V	2	[29] [30]
MSK5978RH	M. S. Kennedy	1028	LDO Positive Adjustable Voltage Regulator	Linear Bipolar	L: (NRL10OCT) JP	L: SETs are approximately +/- 150 mV and 40 μs worst-case with a 0.25 Ω, 22 μF tantalum capacitor. No destructive effects observed.	16, 5.6, 5.0, 3.9, 2.2V	2	[31]
S2803R3S	International Rectifier	0324	DC-DC Converter	Hybrid	L: (NRL10MAY) AS	L: One photon absorption; SETs observed at ~+/-150mV, 100us.	3.3V	2	[32]
SMSA2815S	Crane	0617	DC-DC Converter	Hybrid	L: (NRL10MAY) AS	L: One photon absorption; SETs observed at ~+160mV and -192mV, 100us.	+/-15V	2	[33]
FPGA:									
A3PE3000	Actel	0832	FPGA	CMOS	H: (TAMU10MAY) MB	H: SEL LET _{th} > 57 @ room temperature; No Mitigation and LTMR 1.0 < SEU LET _{th} < 2.8; DTMR: 8.6 < SEU LET _{th} < 12.0	3.3V I/O; 1.5V Core	6	[34] [35]
RTAX2000S	Actel	0311; 0838; 0526;	FPGA	Antifuse Tech- nology/ CMOS	H: (TAMU10MAY; TAMU10AUG; TAMU10DEC) MB	H: SEL LET _{th} > 80 @ room temperature; Counters @120MHz: 1.0 < SEU LET _{th} < 3.0; Shift Registers @160MHz; 3.0 < SEU LET _{th} < 6.0	2.5V, 3.3V I/O; 1.5V Core	4	[35] [36]
ACSPD60	Achronix	0921	FPGA	CMOS	H: (TAMU10MAR) MB; P (IU10MAR) MB	H: Configuration LET _{th} < 1; Tests that contained a large amount of bit upsets also experienced sharp current jumps. This is more than likely not SEL but many configuration bits in the wrong state causing contention within the fabric. P: SEU σ = 2x10 ⁻³ cm ² /device @ 45 MeV	3.3V I/O; 1V Core	1	[37] [38]
XC6SLX16	Xilinx	0929	FPGA	45nm CMOS	P (IU10MAR) MB	P: No SEL observed at room temperature proton energy <200 MeV; Configuration SEU σ = 1x10 ⁻¹⁴ cm ² /bit @ 63 MeV	2.5V I/O; 1V Core	2	[39]

Part Number	Manufacturer	LDC	Device Function	Technology	Particle: (Facility/Date) P.I.	Test Results LET in MeV·cm ² /mg σ in cm ² /device, unless otherwise specified	Supply Voltage	Sample Size (Number Tested)	Reference
Linear and Analog Devices:									
LTC2054HV	Linear Technology	1047T	Operational Amplifier	CMOS	H: (TAMU10OCT) JP	H: SEL LET _{th} > 77 @ 65°C	+/- 5V	4	[40]
HS9-1840ARH	Intersil	0902	16-channel Analog Multiplexer	CMOS	L: (NRL10MAY) MiC	L: SETs typically under ~100mV WC transient 250mV.	5V	2	[41]
ISL28196	Intersil	0724	Voltage comparator	CMOS	L: (NRL10MAR) DC	L: Laser tested at 25°C to 75°C. Maximum amplitude exceeds 5 V (saturated by supply limits) with full width half max pulse width of ~ 10 μ s. SETs decreased in magnitude with increasing temperature.	5V	5	[42]
LTC6400-20	Linear Technology	0746; 0705	Differential Amplifier	SiGe BiCMOS	L: (NRL10MAR) DC; P (IU10MAR) DC/JP	L: Operating at 500MHz. The SETs distort the sinusoidal signal for 1 to 2 clock periods. SETs are less significant than those from heavy-ion test. TID-irradiated part showed higher sensitivity than the virgin part. P: Operating at 200 MHz. 200 MeV protons caused small distortions to the sinusoidal signal, affecting 1/2 clock period. Changes in the SET σ with fluence likely due to deviations from a Poisson distribution and/or part-to-part variation.	3V	2	[43] [44]
Power MOSFET/Transistor:									
SiB455EDK	Vishay Intertechnology	9QZ	12 V p-type Power MOSFET	Trench	H: (TAMU10AUG) JML	H: Primary failure mode: SEGR. Angle: 2° worse than 45° and 60°. 2° max pass/first fail V _{ds} : Kr (LET 28) pass -12V at 0V _{gs} , -11/-12V at 2V _{gs} , -7/-8V at 5V _{gs} ; Ag (LET 43) -11/-12V at 0V _{gs} , -6/-7V at 5V _{gs} .	0, 2, 5V _{gs}	20	[45]
Si7431dp	Vishay Intertechnology	ZZ W54B & AB W08B	200 V p-type Power MOSFET	Trench	H: (LBNL11JAN, LBNL11MAR) JML	H: Primary failure mode: SEGR. Kr (LET 25) pass -200V _{ds} at 0-5V _{gs} , fail -110V _{ds} at 10V _{gs} ; no failures at 45° or 60° at 0-10V _{gs} . Ag (LET=48, 0° data only) max pass/first fail V _{ds} : -150/-155V at 0V _{gs} , -90/-100V at 5V _{gs} , -30/-40V at 10V _{gs} .	0, 5, 10V _{gs}	22	[46]
SCF9550	Semicoa	Engineering Samples	450 V n-type power MOSFET	VDMOS	H: (TAMU10DEC) JML	H: Ag (LET 42) pass/fail 150V/170V.	0V _{gs}	3	[47]
2N7270	Semicoa	Engineering Samples	500 V n-type power MOSFET	VDMOS	H: (TAMU10AUG) JML	H: Tests conducted on multiple process variations in support of product development.	0V _{gs}	13	[48]
STRH100N10F SY3	STMicro	Engineering Samples	100 V n-type power MOSFET	VDMOS	H: (TAMU10AUG, TAMU10DEC) JML	H: Primary failure mode: SEGR. Kr (LET 28) pass 100V _{ds} at 0V _{gs} ; Kr (LET 31) max pass/first fail V _{ds} 80/85V at 0V _{gs} ; Ag (LET 42) max pass/first fail V _{ds} : 50/55V at 0V _{gs} , 35/40V at 5V _{gs} .	0, 5V _{gs}	18	[49]

Part Number	Manufacturer	LDC	Device Function	Technology	Particle: (Facility/Date) P.I.	Test Results LET in MeV·cm ² /mg σ in cm ² /device, unless otherwise specified	Supply Voltage	Sample Size (Number Tested)	Reference
Miscellaneous:									
STAR-250NDR	Cypress	Custom test vehicle	Active Pixel Sensor	CMOS	H: (TAMU10AUG) JP	H: SEL LET _{th} > 77 @ 65°C	3.5, 5.0, 5.5, and 6.0V	2	[50]
PCM A33	Numonyx	0930	Nonvolatile Memory	90 nm chalcogenide PCM	H: (TAMU10MAY) HK/TO	H: SEL LET _{th} < 31.9; SEL σ > 2.6x10 ⁻⁵ cm ² ; PCM's SELs were from control circuitries.	3V	8	[51]
NAND04GW3B 2DN6	Numonyx	0831	4G NAND Flash Memory	73 nm CMOS	H: (TAMU10MAY) TO	H: SEL LET _{th} > 56; SEFs observed (control logic errors on nearly every dynamic mode shot); Bit error σ < 1x10 ⁻¹⁰ cm ² /bit.	3.3V	2	[52]
K9F8G08U0M	Samsung	0807	8Gbit NAND Flash Memory	60 nm CMOS	H: (TAMU10DEC) TO	H: Current Spike Experiment at high LETs	3.3V	4	[53] [54]
RAM-3+	Mini-Circuits	0918	MMIC Amplifier	InGaP	L: (NRL10FEB) JP	L: Sensitive to SETs. No destructive effects observed.	5V	2	[55]
RAM-6+	Mini-Circuits	0927	MMIC Amplifier	Silicon Bipolar	L: (NRL10FEB) JP	L: Sensitive to SETs. No destructive effects observed.	3.5V	2	[56]
HMC422 (Generic PN); HMC4562G8 (Engineering PN); HMC4563G8 (Flight PN)	Hittite Microwave Corp.	JX22 (24th week of 2009)	GaAs MMIC mixer with integrated LO amplifier	MESFET	L: (NRL10JAN) JP	L: The 590 nm laser pulse produced SETs under all conditions tested for both DC and down conversion from 1530 MHz to 30 MHz. Transients < 0.5 V for DC and AC input conditions on RF and LO, with pulse width ~1 ns at 10% of the peak voltage.	3V	2	[57]
MT29F4G08AA AWP	Micron	0748	4Gbit NAND Flash Memory	73 nm CMOS	H: (TAMU10DEC) TO; L: (NRL11MAR) TO	H: Current Spike Experiment at high LETs; L: (NRL11MAR) Sensitive areas were identified.	3.3V	5	[53] [54] [58]
IS705RH	Intersil	002	Power On Reset Circuit	CMOS	H: (TAMU10MAY) MIC; L: (NRL10MAY) MIC	H: 2.8 < SET LET _{th} < 8.6; L: SET triggers Reset.	15V	2	[59]
CMOS Test Vehicle:									
Test Vehicle	IBM	Custom test vehicle	Latches	45 nm SOI CMOS	H: (TAMU10MAR) (LBNL10JUN) JP; P: (IU10MAR) (UDC10JUN) JP; Part was tested throughout 2010/2011 at the IBM VdG facility.*	H: SEU LET _{th} < 0.5. No destructive effects observed. TAMU, LBNL, and IBM VdG* results agree. P: SEU LET _{th} < 1; Sensitive to low-energy protons.	0.6-1.0V	3	[60]
Test Vehicle	IBM	Custom test vehicle	Latches	32 nm SOI CMOS	H: (LBNL11JAN) JP; P: (UDC10OCT) JP; Part was tested throughout 2010/2011 at the IBM VdG facility.*	H: SEU LET _{th} < 2. No destructive effects observed. LBNL and IBM VdG results agree.* P: SEU LET _{th} < 2; Sensitive to low-energy protons.	0.7-1.0V	2	[60]
Test Vehicle	Intel	Custom test vehicle	Latches	45 nm CMOS	P: (UDC10OCT) JP	P: Sensitive to low-energy protons. Irradiations conducted below nominal operating voltage.	0.5-0.7V	5	[61]
Test Vehicle	Intel	Custom test vehicle	Latches	32 nm CMOS	P: (UDC10OCT) JP	P: Sensitive to low-energy protons. Irradiations conducted below nominal operating voltage.	0.7V	5	[61]

* The IBM T.J. Watson Research Center has a 3 MV Tandem Van de Graaff accelerator that is used for SEU experiments. The lab has seven beam lines, one of which is dedicated to SEU exposures. The ion sources for the accelerator consist of a sputter source (SNICS) for 1H, 2H, 12C and other beams as well as a RF source (alphatross) used to produce alpha particles (4He). [IBM VdG-Heidelberg]

IV. TEST RESULTS AND DISCUSSION

As in our past workshop compendia of NASA Goddard Space Flight Center (GSFC) test results, each DUT has a detailed test report available online at <http://radhome.gsfc.nasa.gov> [11] describing the test method, SEE conditions/parameters, test results, and graphs of data.

This section contains summaries of testing performed on a selection of featured parts.

A. Vishay SiB455EDK and Si7431DP Commercial Power MOSFETs

This study was undertaken to determine the SEGR and SEB susceptibility of Vishay's commercial p-type trenchFET® power MOSFETs under heavy-ion irradiation. The SiB455EDK is a 12 V, 9 A p-channel trench MOSFET from Vishay's Gen III line. The Si7431DP is a 200 V, 2.2 A p-channel trench MOSFET introduced in 2005. Past reports of trench power MOSFETs have focused on n-channel devices and the substantial degradation from localized dose deposited by heavy ions [63] [64]. We believe the test reported here is the first to evaluate the suitability of p-channel trench MOSFETs for space applications.

The SiB455EDK tests were conducted in air at three different angles (2°, 45°, and 60°); the Si7431DP tests were conducted in vacuum at normal beam incidence, with additional tests at 45° and 60° under 1230 MeV Kr only. Each sample was biased at one of three gate-source voltage biases, and the drain-source voltage was incremented between beam runs until device failure was observed. Currents were monitored at the gate and drain nodes during testing, and a post-irradiation gate stress test was performed following each beam run. Failure was defined as the gate current exceeding the vendor specified maximum leakage current, and/or a sudden, sustained increase in drain current. In addition, the gate threshold voltage was measured following each beam run to monitor for dose effects. No dosing effects were seen during heavy-ion testing, and as reported in [2], the SiB455EDK showed a TID tolerance to more than 100 krad(Si) with Co60 irradiation.

The primary failure mode of the SiB455EDK was SEGR, although in some samples irradiated at 2° a SEB signature was detected that also resulted in gate damage. The SEE response curve for the 2° angle of incidence is shown in Fig. 1; the data obtained at higher angles are plotted in Fig. 2.

The primary failure mode of the Si7431DP was SEGR. The SEE response curve for data taken at normal incidence is shown in Fig. 3. In this figure, the krypton data point at 10 V_{gs} reflects the lowest failure V_{ds}; two samples passed at -120 V_{ds}, failing at the next bias step, but the third sample failed during the first beam run at -110 V_{ds}. At all three V_{gs} biases, no failures were detected at 45° and 60° angles of 1230 MeV krypton beam incidence.

The results suggest that these Vishay commercial p-type trench power MOSFETs are a consideration for space applications. [45] [46]

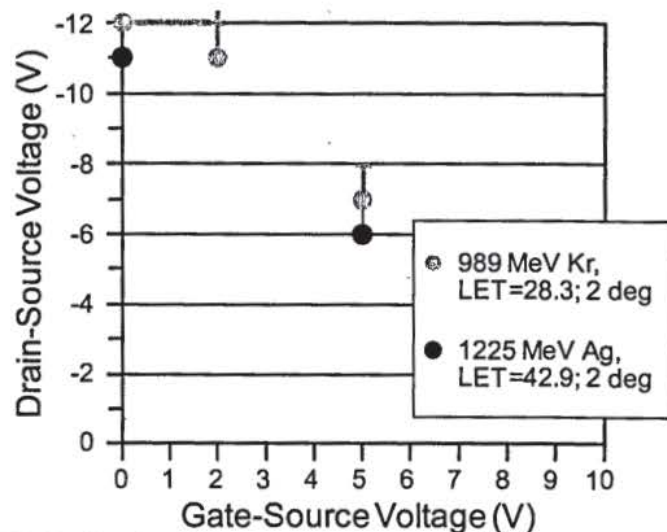


Fig. 1. Vishay SiB455EDK Commercial Power MOSFET SEE response curve for the 2° angle of incidence.

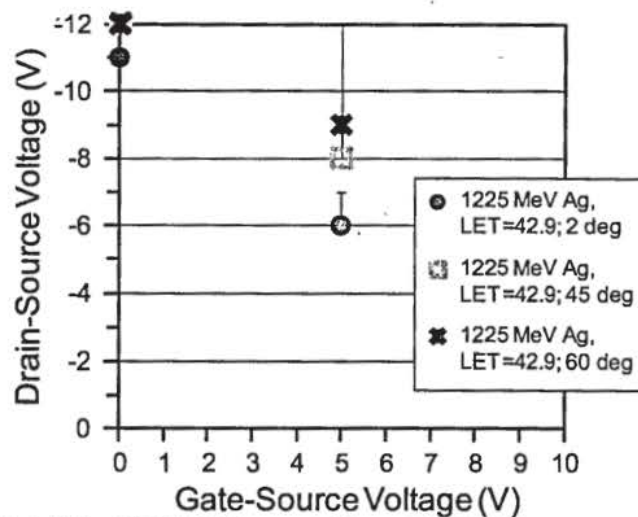


Fig. 2. Vishay SiB455EDK Commercial Power MOSFET SEE response curve for the higher angles of incidence.

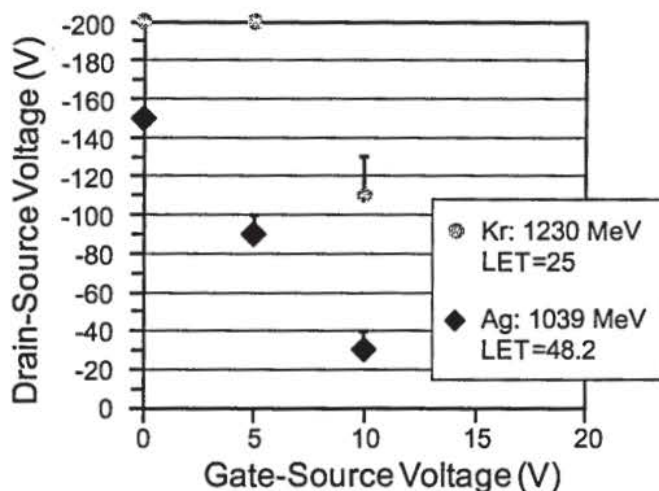


Fig. 3. Vishay Si7431DP Commercial Power MOSFET SEE response curve at normal incidence.

B. PE9915X Monolithic Point-of-Load Switching Regulator

The PE9915X is a series of monolithic point-of-load (POL) switching regulators fabricated in Peregrine's UltraCMOS® technology, which utilizes a Silicon-On-Sapphire (SOS) process. We examined the PE99151 (2 A) and the PE99155 (10 A) versions. The output voltage is adjustable down to 1 V. The manufacturer supplied customized evaluation boards for the test, which consists of external resistors, capacitors, and an inductor. We note that the device has a 1000 μF capacitor at the output.

Three parts were tested at the LBNL facility. The test was performed in a vacuum environment. The application boards were attached to metal plates to facilitate conductive heat sinking. Fig. 4 shows a block diagram of the test setup and Fig. 5 shows the photograph of the device inside the test chamber.

We irradiated the parts with 10 MeV/amu Xe at 0° and 60° for different output load conditions. We observed a few incidences of sharp voltage spikes, with magnitudes of 0.4 to 0.6 V and durations on the order of 10s of nanoseconds. However we believe that these signatures originated from sources external to the device and test board. The resonating frequency of the pulse and the short duration suggest that the voltage spikes were likely caused by noise associated with the vacuum chamber and/or equipment in the irradiation room.

We also observed an incidence where the input supply current fell rapidly, which caused an output regulation failure, as shown in Fig. 6. However we believe that the event was not caused by a single particle strike. It may have been caused in part by device overheating, as conductive heat-sinking becomes inefficient in a vacuum environment. The parametric degradations from accumulated dose may have also contributed to the current drop. We observed parametric shifts during electrical characterization approximately 48 hours after the heavy-ion test. Additional tests in air, eliminating the heat sinking issues were performed to verify the cause of the event. [17]

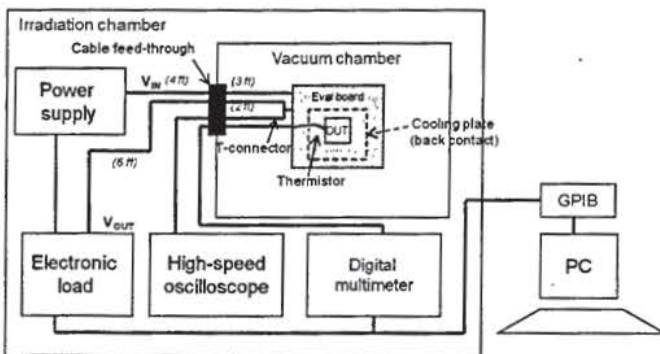


Fig. 4. Block diagram of the testing setup for the PE9915X Monolithic Point-of-Load Switching Regulator.

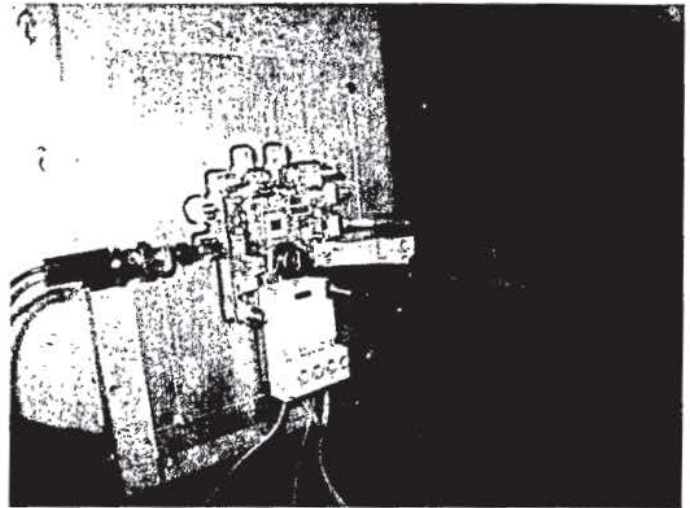


Fig. 5. Photograph the PE9915X test board mounted with heat sink in the irradiation chamber.

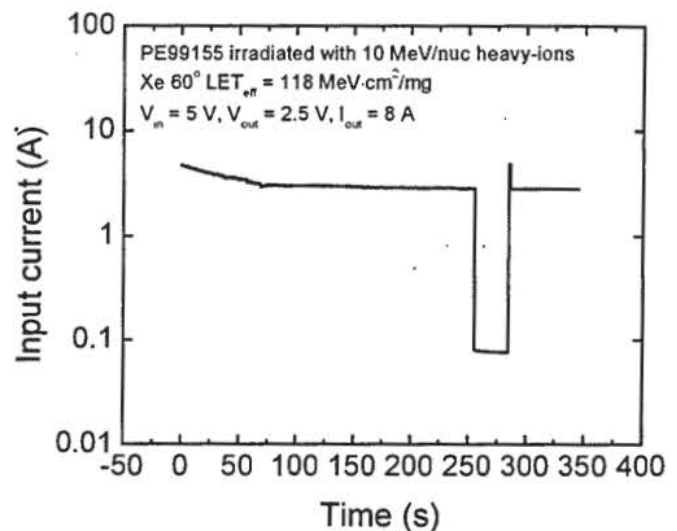


Fig. 6. Input current vs. time for the PE99155, operating with $V_{out} = 2.5 \text{ V}$ and $I_{out} = 8 \text{ A}$, irradiated with Xe at 60° with an effective LET = 118 MeV·cm²/mg, for 10 MeV/nuc heavy-ions.

C. Hittite HMC422 Double-Balanced Mixer Integrated Circuit

The Hittite HMC422 is a double-balanced mixer integrated circuit with integrated local oscillator (LO) amplifiers fabricated as a monolithic microwave integrated circuit in a gallium arsenide (GaAs) process. This mixer can operate as an upconverter or downconverter between 1.2 GHz and 2.5 GHz. With the integrated LO amplifier, the mixer requires an LO drive level of only 0 dBm, and requires only 30 mA from a single positive 3 V rail. The mixer has 8 dB of conversion loss, an input P_{1dB} of +8 dBm and an input third order intercept point of +15 dBm at 2 GHz. The device was monitored for analog single-event transients (ASETs) on the IF output and for any destructive events induced by exposing it to a pulsed laser beam at the NRL laser test facility. The application being tested was used to downconvert a 1530 MHz CW signal to 30 MHz continuous wave (CW) by supplying inputs to RF and LO while monitoring IF with the oscilloscope.

The device was prepared for test by depotting the topside of the plastic package via acid etching and then mounting it onto a Hittite evaluation board (part number 104813) that uses a Rogers 4350 substrate and 50 Ω signal line impedance. A finished 1 inch by 1 inch square test board is shown in Fig. 7.

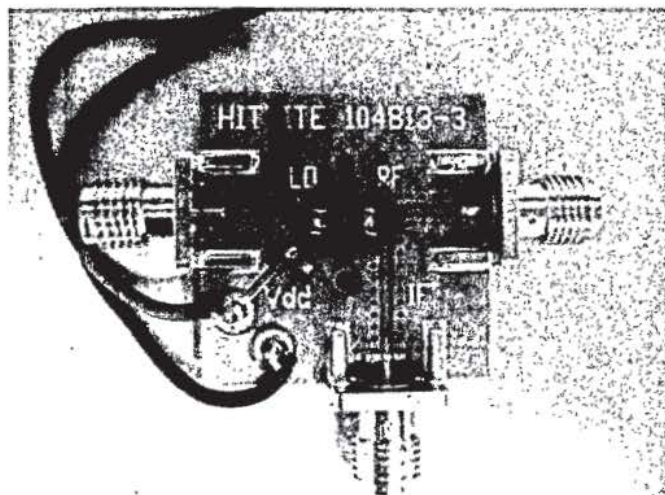


Fig. 7: Photograph of completed printed circuit board ready for pulsed laser testing. The device under test is in the center of the board and the surface-mount connectors on the three edges are SMA type. The V_{dd} power supply (3 V) as well as the LO, IF, and RF signal lines are marked.

The tests were performed on two devices at the NRL using their single-photon absorption (SPA) setup. This system has been discussed in several refereed publications and will not be covered in detail [65] [66] [67]. The device lot date code was JX22. The DUT was packaged in a plastic MSOP-8 package with a copper alloy lead frame. The test setup consisted of laptop running LabVIEW for instrument control and data capture, a Tektronix DSA72004B digital storage oscilloscope (20 GHz, 50 GS/s), two HP 83712B synthesized CW generators, and an Agilent N6702A MPS mainframe 4-channel power supply. A separate function generator specific to the NRL test facility was used to synchronize the two GSFC function generators to the delivery of the laser pulse so that different points within the clock period could be sampled. The two function generators had their 10 MHz synchronization lines tied to the NRL function generator sync I/O. This allowed the laser pulse firing to be used as the trigger source for the oscilloscope enabling the laser pulse to move throughout all 2π of the CW input on RF and LO.

The laser was focused onto the HMC422 die and scanned across the surface to produce transients on the IF output. This was done for two different input (RF and LO) conditions: 1) biased operation with the RF and LO inputs terminated, and 2) biased operation with RF and LO inputs stimulated with 1530 MHz and 1500 MHz CW sine wave signals at 0 dBm. This was not an application specific test, but the input frequencies were relevant for the end users. The parameters varied were the RF and LO input conditions and the laser pulse energy. Transients were captured for all test conditions and are shown in Fig. 8.

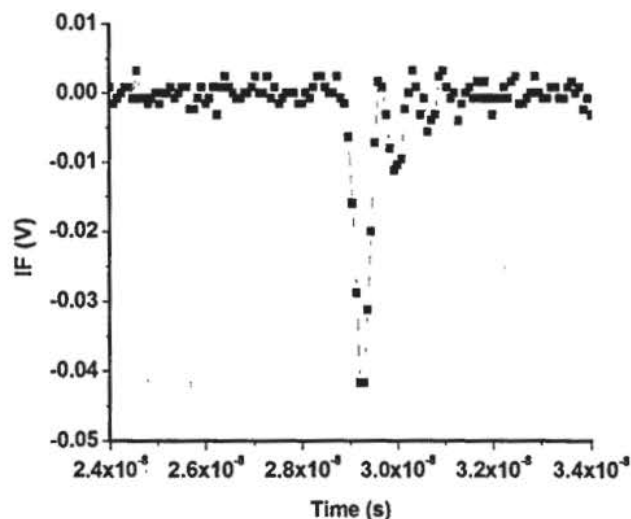
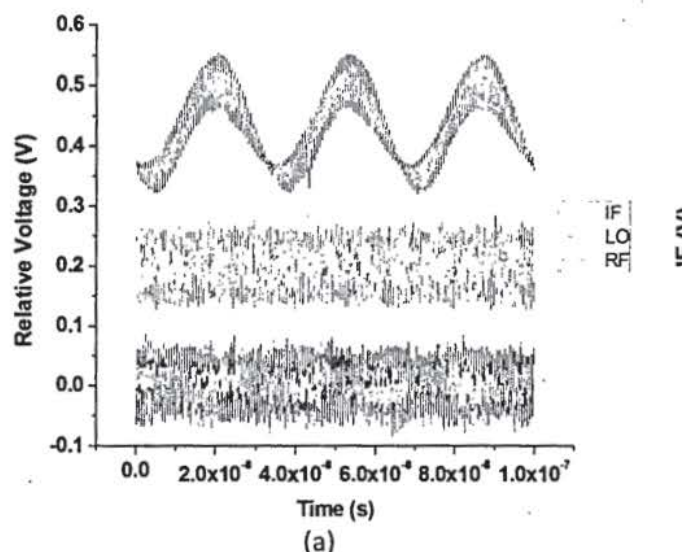


Fig. 8: Example ASET for DC input conditions on RF and LO. The GaAs MESFETs in the center of the die were the only source of transients – the LO amplifier did not appear to contribute. All transients are negative. These transients were recorded at a laser pulse energy of approximately 33 pJ.

The Hittite HMC422 tested here showed transients less than 0.5 V in amplitude for both DC and AC input conditions on RF and LO up to a laser pulse energy of 33 pJ. The transients widths, measured at 10% of the peak voltage, were approximately 1 ns. The DC input condition ASETs measured on IF appeared to be simply superimposed on the IF signal and caused no further distortion during AC input conditions. The amplitude and width remained unchanged as shown in Fig. 9.

GaAs technologies generally suffer from large single-event cross sections due to large charge collection efficiencies and high carrier mobility. These tests seem to indicate that the response saturated quickly with increasing laser pulse energy.[57]



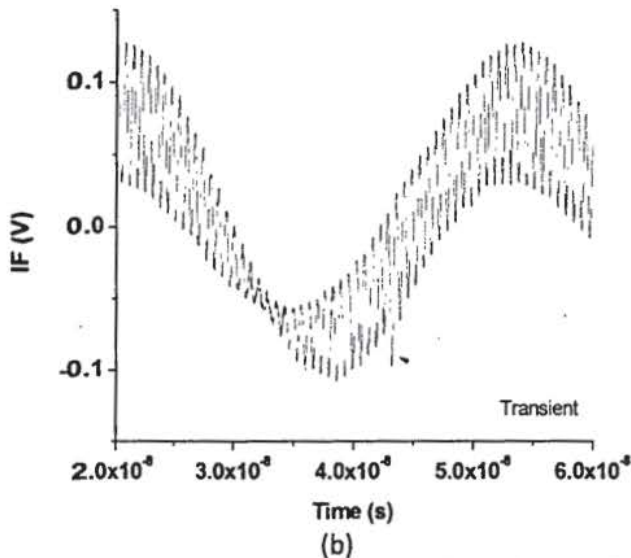


Fig. 9: These figures show AETs for AC RF and LO input characteristics at a pulse energy of 33 pJ. (a) shows an AET on IF as well as the raw RF and LO signals from the CW generators; (b) shows a zoomed image of the AET from the top trace of (a). Note that the voltages shown in (a) are arbitrary and simply relative within each trace's range – the data were stacked to show them on the same abscissa.

D. MSK5978RH LDO Positive Adjustable Regulator

This study was undertaken to determine the ASET susceptibility of the M. S. Kennedy MSK5978RH low dropout (LDO), positive, 0.7 A, adjustable linear regulator. The device was monitored for transients on the voltage output while exposing it to a pulsed laser beam at the NRL laser test facility.

The sensitive structure within the MSK5978RH is the Linear Technology RH3080, which integrates a PNP pass transistor and the regulation control loop circuitry onto a single die; this makes this part fundamentally different from previous RH1573K/pass transistor combinations in other LDO regulator offerings from M.S. Kennedy and Linear Technology. A photograph of the die is shown in Fig. 10.

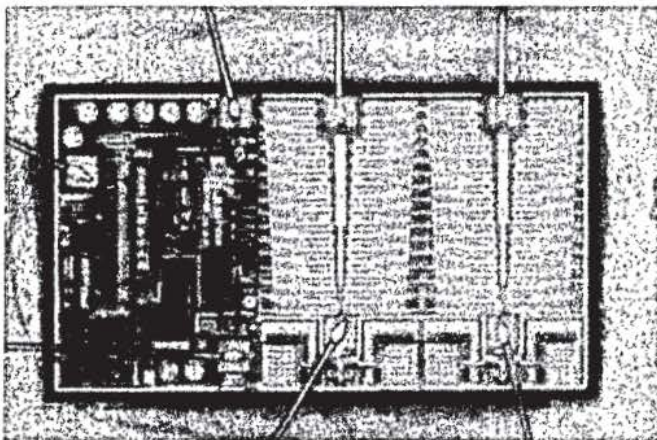


Fig. 10: MSK5978RH photomicrograph of the RH3080 die inside the hybrid package. The pass transistor is on the left, while the controller circuitry (current source, voltage follower, etc.) is on the right. The pass transistor is not sensitive to SETs, but the controller circuitry can produce ASETs. This was the primary target of the pulsed laser.

We tested the MSK5978RH at the NRL using a 590 nm

wavelength laser pulse with a pulse width of approximately 1 ps. Both 100x and 10x objectives were used to focus the beam onto the surface of the die yielding spot sizes between 1.2 and 12 μm in diameter. The difference in spot size did not affect the transient behavior. The pulse energy was maintained at 4.6 pJ, which is sufficiently conservative for a worst-case analysis.

The laser spot was scanned across the controller circuitry and the ASETs were captured and recorded using a 500 MHz oscilloscope (Tektronix MSO4054B). The application conditions required that we test the LDO regulator under several input bias and output load conditions. Fig. 11 shows the characteristic amplitude and width for ASETs under two different conditions: 1) 16 V input, 15 V output, and 150 mA load; and, 2) 2.2 V input, 1.5 V output, and 180/500 mA loads. In addition to 0.1 and 1.0 μF ceramic surface-mount capacitors, the output was loaded with a 22 μF tantalum capacitor (Kemet T495D226K035ATE250) with an equivalent series resistance of approximately 0.25 Ω .

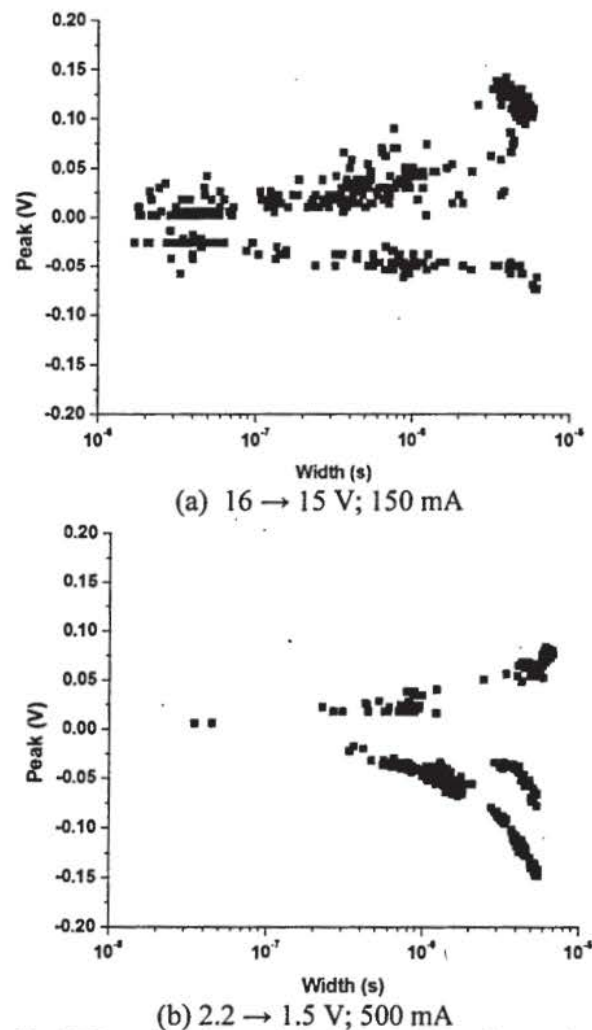


Fig. 11: ASET transient characteristics for two different input and output conditions. The voltage on the ordinate is the peak amplitude of the ASET, which is the larger of the two excursions from 0.0 V if the ASET is bipolar. The width is evaluated at 10% of the peak voltage.

As with other M. S. Kennedy LDO regulators, this one is sensitive to ASETs and may require filtering techniques to reduce the transient amplitude at the expense of increasing the transient width. The ASETs reported here are application-specific and are also a function of the radiation source used; a different setup and a heavy ion source would yield different ASET behavior. However, given its smaller size due to increased integration and lower heat dissipation, it may be an attractive option for certain applications. [31]

E. MT29F4G08AAWP Micron 4Gbit NAND

In an effort to determine which regions on the die cause the high currents observed when testing at the TAMU Cyclotron, we conducted tests using the NRL pulsed laser on the MT29F4G08AAWP Micron 4Gbit NAND. We used single photon absorption, shining 590 nm (green) light on the front surface of the Micron 4G NAND flash memory. In Fig. 12, we show the results of the pulsed laser test at NRL. Light spots indicate locations where high current, 80 mA or more, was observed. Dark spots indicate locations where SEFIs, without high current, were observed. There are 38 locations where high currents were triggered by the laser, including almost anywhere in the peripheral control logic. Note, however, that there are no high current events in the regions believed to be the charge pumps (white rectangles). This result is very difficult to reconcile with the conclusion in [68, 69], that the high currents are coming from the charge pumps. [53, 54, 58]

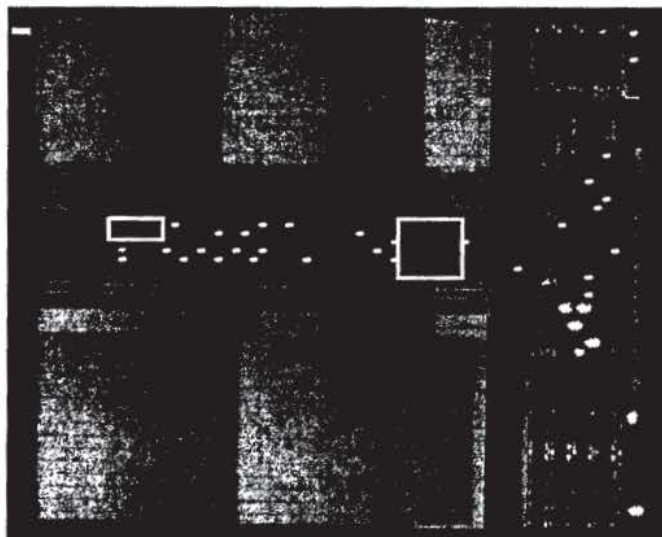


Fig. 12. The red spots indicate locations where high current (>80 mA) was observed. Other colors indicate different kinds of SEFIs, without high current.

V. SUMMARY

We have presented current data from SEE testing on a variety of mainly commercial devices. It is the authors' recommendation that this data be used with caution. We also highly recommend that lot testing be performed on any suspect or commercial device.

VI. ACKNOWLEDGMENT

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